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Thermal Macro-Modeling and Safe Operating Area Analysis of MOSFETs

M. Sudais Khan, Yaseer A. Durrani
Electronics Engineering Department, University of Engineering and Technology, Taxila, Pakistan
*__Correspondence__: M. Sudais Khan; 22-ms-enc-05@students.uettaxila.edu.pk

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Thermal dissipation in electronic circuits is always an important design constraint. Excessive heat can degrade component performance, reduce lifespan, and in severe cases, cause permanent failure. This paper uses the thermal modeling approach at the circuit level and focuses on the Safe Operating Area (SOA) of MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors). The SOA defines the operational limits of MOSFETs by considering the power dissipation to prevent thermal runaway and device failure. In the area of power electronics, it is important to ensure the reliability and efficiency of circuits under different thermal conditions. In this paper, the thermal behavior of MOSFETs is modeled considering factors such as ambient temperature, gate capacitance, PCB (printed circuit board) thermal dissipation, and heatsink addition. This research highlights the importance of thermal design principles in predicting the junction and case temperatures of MOSFETs under various operating conditions. This systematic approach to thermal macro-modeling is crucial for optimizing the performance and reliability of electronic circuits, particularly in high-power applications where thermal management is a critical concern.

Keywords: Thermal Modeling, Power Electronics Circuits, Ltspice, Safe Operating Area, Mosfets

Introduction:

Electronic systems help us in our daily lives in many ways. The next-generation power electronic devices like MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors, Figure 1 can help us to reduce power dissipation. These devices generally offer superior performance, higher efficiency, and greater reliability as compared to the traditional silicon-based devices. In such devices, unexpected problems such as inadequate thermal management may affect their reliability. Therefore, it is crucial to handle thermal design issues properly. This research provides the basics of thermal design, focusing on semiconductor parts such as transistors and integrated circuits (ICs) used in electronic equipment. By minimizing these resistances, the junction temperature (T_J) is lowered, which improves the reliability and performance of the IC. An effective thermal design includes selecting suitable heatsinks, designing efficient airflow paths, and using thermal interface materials to enhance heat dissipation.

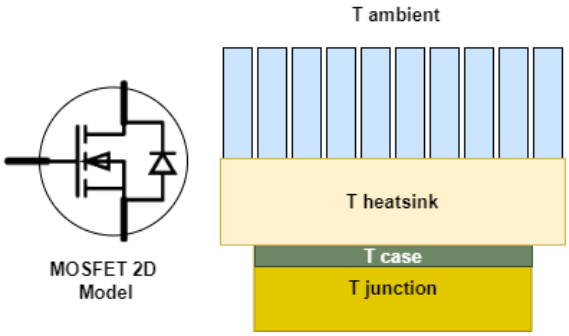


Figure 1. MOSFET Physical Structure

Many researchers have addressed the challenge of managing thermal issues in power electronics-related circuits. The Cauer network Figure 2 can be used to model the thermal behavior of MOSFETs effectively. By representing the MOSFET and its surrounding components (like the PCB and heatsink) with a Cauer network, engineers can simulate and analyze how heat is distributed and dissipated throughout the system [1].

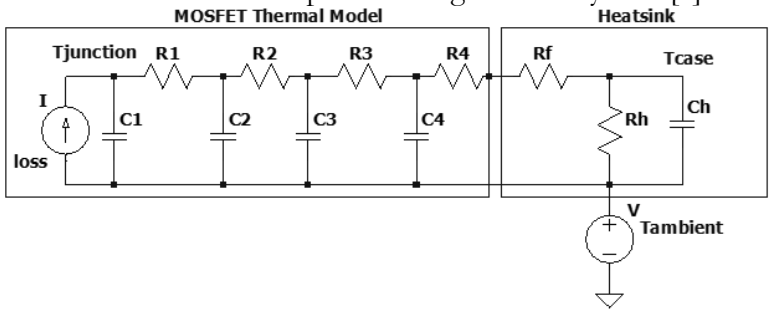


Figure 2. MOSFET Thermal Model (Cauer)

The temperature of the environment is referred to as T_A (ambient temperature) Which is the minimum temperature at which the device operates. Maximum Junction Temperature or (T_{Jmax}) refers to the highest temperature at which the junction of a semiconductor device, i.e, a transistor or integrated circuit, can safely operate without risking damage or degradation to the components. The junction temperature of the device can be lowered by adding a heatsink, cooling pads, or via PCB thermal dissipation [2][3].

Objectives:

1. To study the feasibility of thermal macro-modeling at the circuit level for MOSFET.
2. To analyze the Safe Operating Area (SOA) for assessing MOSFET durability in high-stress scenarios.
3. To optimize thermal management solutions to prevent overheating and ensure device longevity.

4. To investigate the impact of thermal resistance on MOSFET performance and operating limits.
5. To enhance hot swap circuit designs by integrating thermal and SOA information.

Novelty Statement:

This study presents a compact and simulation-ready thermal macro-model for MOSFETs that integrates both electrical and thermal characteristics, enabling accurate Safe Operating Area (SOA) analysis using LTSpice. Unlike conventional approaches that rely solely on empirical SOA charts or complex finite element simulations, this method offers a practical and reusable modeling framework suitable for system-level thermal evaluation, thereby bridging the gap between device-level behavior and circuit-level design validation.

Research Flow:

The flowchart Figure 3 outlines the systematic methodology adopted for thermal macro-modeling and safe operating area (SOA) analysis of MOSFETs. It begins with the selection of an appropriate MOSFET model, followed by the extraction of key thermal parameters. These parameters are then used to develop a thermal macro-model, which is simulated in LTSpice to analyze the device's thermal behavior. Finally, the model's performance and SOA are validated using experimental data or datasheet references to ensure accuracy and reliability of the proposed approach.

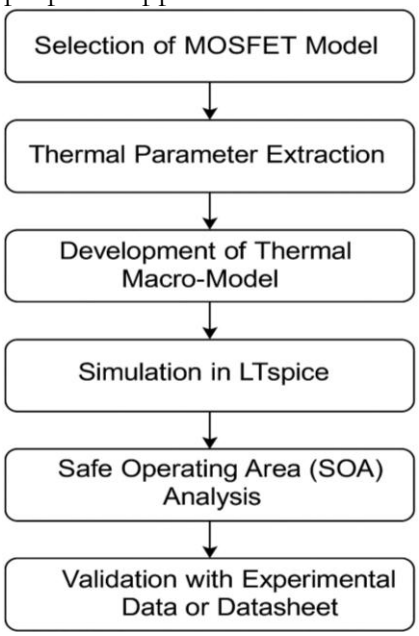


Figure 3. Methodology Flowchart

Methodology:

Thermal Resistance:

Thermal resistance measures the difficulty of heat conduction through a material or between two points. Thermal resistance is calculated by dividing the temperature difference between two points by the heat flow between them (heat flow per unit time) [4].

Mathematically, thermal resistance R_{th} is expressed as:

$$R_{\text{th}} = \frac{T_1 - T_2}{P} = \frac{\Delta T}{P} \quad (1)$$

Where T_1 and T_2 Are the temperatures at two different points, ΔT is the temperature difference between these points and P is the heat flow or the power dissipated between the points.

Thermal resistance is also similar to electrical resistance. The basic formulas for thermal calculations can be treated similarly [5]. Table 1 summarizes the relationships between electrical and thermal parameters.

Table 1. Electrical and Thermal Equivalent Quantities

Parameter	Electrical	Thermal
Difference	Potential difference ΔV (V)	Thermal difference ΔT (°C)
Resistance	Resistance R (Ω)	Thermal resistance Rth (°C/W)
Flow	Currently I (A)	Heat flow P (W)
Equivalent Expression	$\Delta V = R \times I$	$\Delta T = Rth \times P$

To lower the thermal resistance, one should increase the object's surface area or choose a material with high emissivity. There are three main temperatures related to MOSFET: junction temperature, case temperature, and ambient temperature. To calculate the temperature difference between the junction temperature T_J and the ambient temperature T_A, thermal resistance equation can be used provided the thermal resistance of the paths and the power loss of the IC are known. This equation helps in determining how much the junction temperature will rise above the ambient temperature due to the power dissipated by the IC [6].

$$\Delta T = R_{\text{th}} \times P \quad (2)$$

Where ΔT Is the temperature difference, R_{th} Is the thermal resistance, and P is the power dissipation.

The equation can be further rearranged, and the temperature of the silicon die can be calculated as:

$$T_{\text{JUNCTION}} = T_{\text{AMBIENT}} + \theta_{\text{JA}} \times \text{Power} \quad (3)$$

$$T_{\text{JUNCTION}} = T_{\text{CASE}} + \theta_{\text{JC}} \times \text{Power} \quad (4)$$

Where T_{JUNCTION} is the junction temperature, T_{CASE} Is the case temperature, T_{AMBIENT} Is the temperature of the surroundings, θ_{JA} is the junction-to-ambient thermal resistance and θ_{JC} It is junction-to-case thermal resistance.

The θ_{JA} The value is used to determine the temperature rise from the ambient environment to the MOSFET's silicon die, based on a specific PCB configuration detailed in the datasheet. For instance, with a θ_{JA} of 62 K/W and an ambient temperature of 65°C, the temperature of the die will reach 127°C when the MOSFET dissipates 1W of power. This is essential to ensure that the MOSFET will remain within the safe operating temperature limits. θ_{JC} is often more valuable because it characterizes the MOSFET's behavior independently of the PCB layout [7].

Dissipation and Transfer of Heat in an IC:

Heat transfer, the movement of thermal energy, is essential in both natural and engineered processes [8]. In electronic components, heat is dissipated through conduction, convection, and radiation. Heat generated by the chip (die) is transferred via conduction to parts of the IC package, including the die attach, lead frame, and case. Convection occurs when the PCB and IC package transfer heat to the surrounding air, creating air circulation that promotes cooling. Radiation allows heat to be emitted as electromagnetic waves, dissipating energy to the surrounding environment Figure 4 [9].

Effect of External Cooling:

The PCB layout, airflow, and heatsinks are crucial in an IC. For most modern MOSFETs with exposed metal tabs, the thermal resistance θ_{JA} is largely influenced by the PCB layout rather than the MOSFET itself, although the shape and size of the exposed pad also contribute. Since θ_{JA} is highly dependent on the PCB layout and airflow, the manufacturer's specified θ_{JA} should be used only as a rough estimate. This tells the importance of taking into account the specific layout and cooling conditions in the actual application [10][4]. The junction temperature considering PCB thermal dissipation can be estimated as:

$$T_J = T_A + P_D(\theta_{JC} + \theta_{PCB}) \quad (5)$$

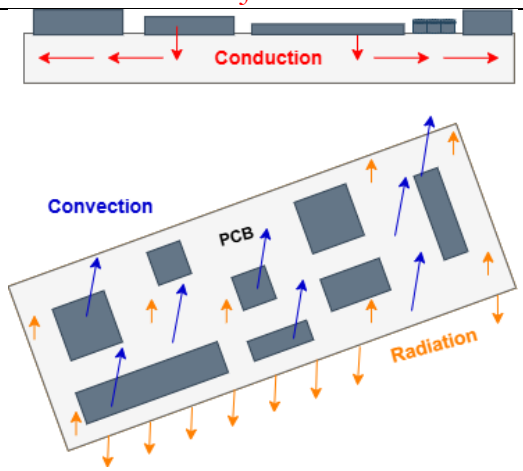


Figure 4. PCB Heat Dissipation

Where $\theta_{PCB} \approx \frac{1}{h_{conv} \times A_{PCB}}$ represents the effective thermal resistance of the PCB, including copper planes and thermal vias (h_{conv} Is the convection coefficient and A_{PCB} It is the area of PCB.

Heatsinks play a vital role in thermal management by increasing the surface area available for heat dissipation. They help in transferring heat away from the MOSFET to the surrounding environment, thereby reducing the junction temperature.

The junction temperature considering the heatsink can be calculated as:

$$T_J = T_A + P_D(\theta_{JC} + \theta_{CS} + \theta_{SA}) \quad (6)$$

Where θ_{JC} Is the thermal resistance from junction-to-case, θ_{CS} is from case to sink and θ_{SA} is the thermal resistance from the sink to the ambient.

Results and Discussion:

The Safe Operating Area (SOA) is a vital parameter in the design and use of MOSFETs. The SOA plot, found in every MOSFET datasheet [11], outlines the maximum time a MOSFET can withstand certain voltage and current conditions without incurring damage [12][13].

Similarly, the transient thermal impedance plot provided in the MOSFET datasheet [11] is essential for understanding the thermal response of MOSFETs to short-duration power pulses.

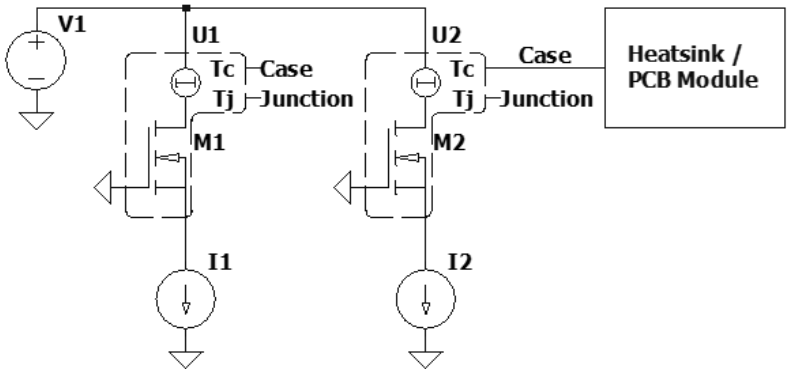


Figure 5. Heatsink and PCB Attachment with MOSFET

In the first part of the simulation, the MOSFET is analyzed first without the external cooling module and then with it attached Figure 5. The power dissipated here is the heat dissipated from the MOSFET and is calculated using equation 4 (θ_{JA} = 62°C/W, θ_{JC} = 0.5°C/W).

After running the simulation, one can observe the junction and case temperatures waveforms in Figure 6, Figure 7, and Table 2.

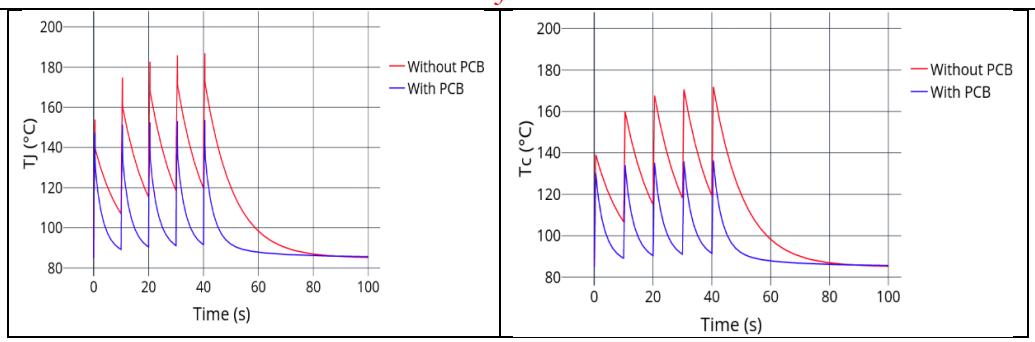


Figure 6. Comparison of Junction and Case Temperatures with and without PCB Thermal Dissipation

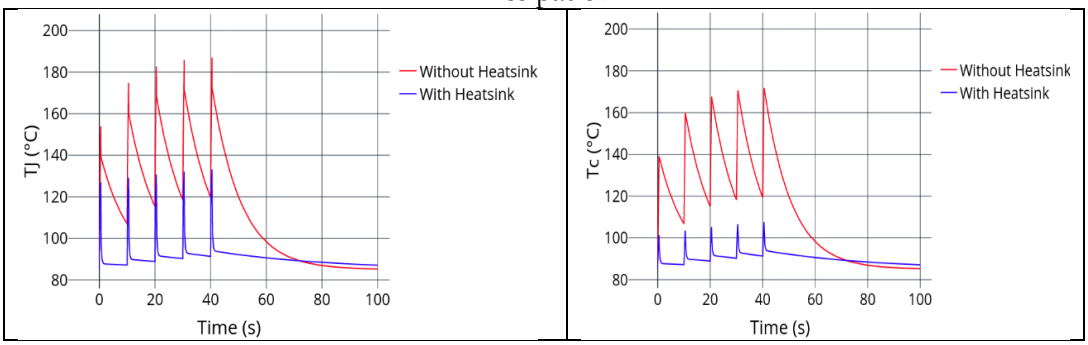


Figure 7. Comparison of Junction and Case Temperatures with and without Heatsink

Table 2. Thermal Performance under Different Conditions

Condition	Junction Temp (°C)	Case Temp (°C)	Power Dissipated (W)	TJ Decrease (%)	TC Decrease (%)
Without External Cooling	186	171	30	-	-
With PCB Thermal Dissipation	153	136	34	17.7%	20.5%
With Heatsink	133	107	52	28.5%	37.4%

Hot Swap Application:

In Hot Swap circuit design Figure 8, one of the biggest challenges is ensuring that a MOSFET operates within its Safe Operating Area (SOA) to prevent damage [3][14]. During normal operation, a short circuit at the output can occur, for example, if a user accidentally drops a paperclip into the chassis. A hot swap circuit (or fuse) can prevent such incidents from causing severe damage or requiring emergency services.

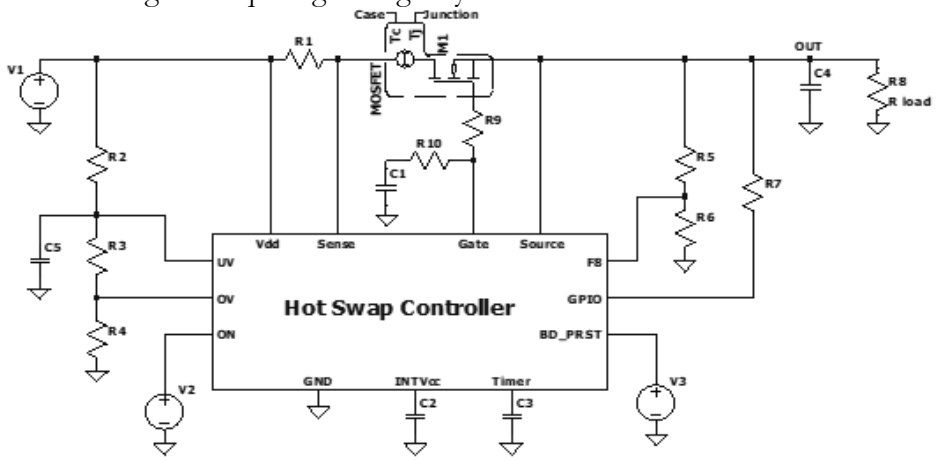


Figure 8. Hot Swap Circuit Diagram

The analysis of the junction and case temperatures in the HotSwap circuit under various conditions reveals key insights into thermal performance. Overall, the results emphasize the importance of controlling gate capacitance, optimizing thermal resistance, and implementing effective cooling strategies such as PCB thermal dissipation and heatsinks to maintain safe operating temperatures in HotSwap circuits Figure 9-13 and Table 3.

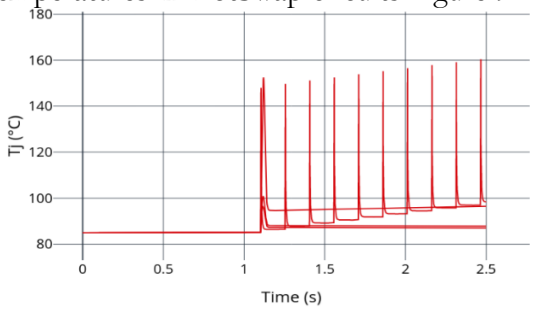


Figure 9. MOSFET Junction Temperature with 85°C Ambient Starting Condition

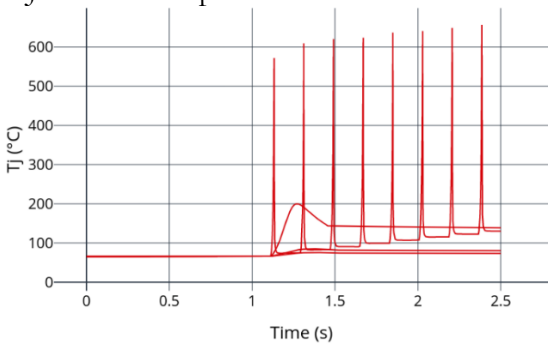


Figure 10. MOSFET Junction Temperature with 100nf Gate Capacitance

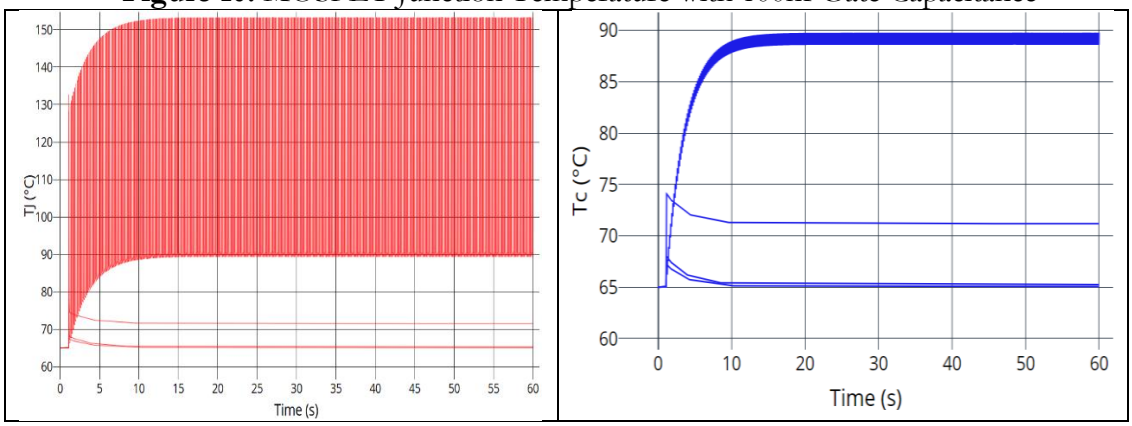
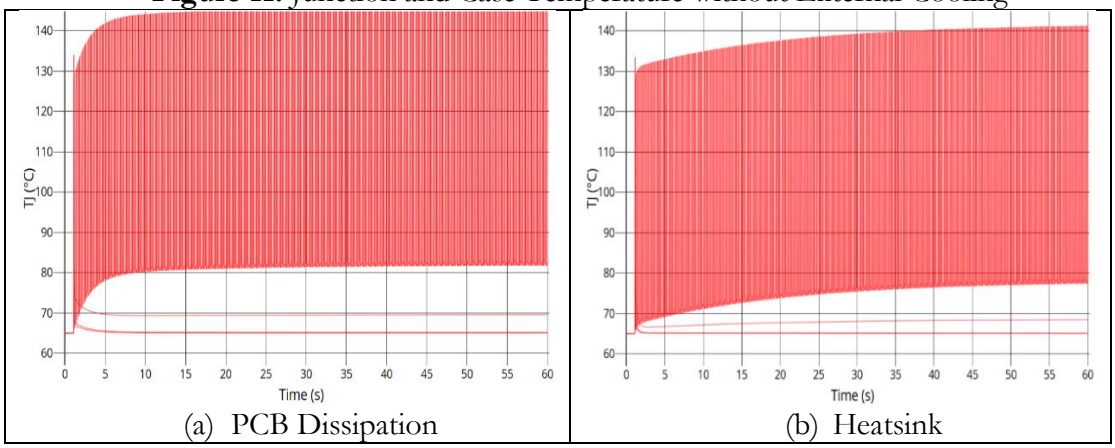
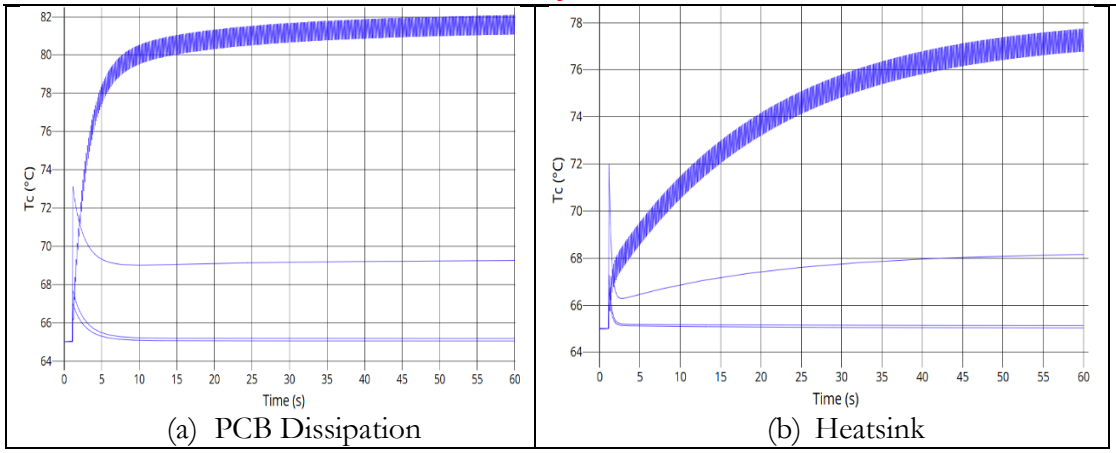


Figure 11. Junction and Case Temperature without External Cooling



(a) PCB Dissipation (b) Heatsink

Figure 12. Junction Temperature with PCB Dissipation and Heatsink



(a) PCB Dissipation (b) Heatsink

Figure 13. Case Temperature with PCB Dissipation and Heatsink

Table 3. Comparison of Junction and Case Temperatures in HotSwap Circuit

Condition	*TJ*-peak (°C)	*TC*-peak (°C)	Duration (sec)	Power Dissipated (W)	*TJ* Decrease (%)	*TC* Decrease (%)
1. Ambient Temperature						
Tambient= 100°C	176	113	2.5	1.3	-	-
Tambient= 85°C	160	98	2.5	1.3	-	-
Tambient= 65°C	140	78	2.5	1.3	-	-
Tambient= 45°C	120	58	2.5	1.3	-	-
Tambient= 25°C	100	38	2.5	1.3	-	-
Tambient= 5°C	80	18	2.5	1.3	-	-
Tambient= -10°C	65	3	2.5	1.3	-	-
Average change in junction temperature = 3.14°C against 1°C of ambient temperature						
Average change in case temperature = 1.37°C against 1°C of ambient temperature						
2. Gate Capacitance (Ambient kept constant at 65°C)						
Gate Capacitance 100 nF	660	142	2.5	-	-	-
Gate Capacitance 75 nF	454	124	2.5	-	-	-
Gate Capacitance 50 nF	304	103	2.5	-	-	-
Gate Capacitance 25 nF	193	86	2.5	-	-	-
Gate Capacitance 10 nF	140	78	2.5	-	-	-
Gate Capacitance 5 nF	126	74	2.5	-	-	-
Average change in junction temperature = 10.94°C against 1nf of gate capacitance						
Average change in case temperature = 5.20°C against 1nf of gate capacitance						
3. RthetaJA Modification (Temperature kept constant at 65°C)						
$R\theta JA$=40	226	161	60	2.4	-	-
$R\theta JA$=25	190	126	60	2.4	-	-
$R\theta JA$=10	153	89	60	2.4	-	-
$R\theta JA$=5	141	77	60	2.4	-	-
Average change in junction temperature = 14.19°C against 1 unit of $R\theta JA$						
Average change in case temperature = 8.34°C against 1 unit of $R\theta JA$						
4. Without External Cooling (RthetaJA kept constant at 10)						
Tambient= 100°C	188	124	60	2.4	-	-
Tambient= 85°C	173	109	60	2.4	-	-
Tambient= 65°C	153	89	60	2.4	-	-
Tambient= 25°C	112	49	60	2.4	-	-

Tambient= 5°C	93	29	60	2.4	-	-
Average change in junction temperature = 5.87°C against 1°C of ambient temperature						
Average change in case temperature = 2.33°C against 1°C of ambient temperature						
5. With PCB Thermal Dissipation						
Tambient= 100°C	181	116	60	3.9	3.7%	6.5%
Tambient= 85°C	165	101	60	3.9	4.6%	7.3%
Tambient= 65°C	145	82	60	3.9	5.2%	7.9%
Tambient= 25°C	106	42	60	3.9	5.4%	14.3%
Tambient= 5°C	86	22	60	3.9	7.5%	24.1%
Average change in junction temperature = 5.084°C against 1°C of ambient temperature						
Average change in case temperature = 1.93°C against 1°C of ambient temperature						
6. With Heatsink Attached (Rtheta = 10)						
Tambient= 100°C	176	112	60	3.6	6.4%	9.7%
Tambient= 85°C	161	97	60	3.6	6.9%	11.0%
Tambient= 65°C	141	77	60	3.6	7.8%	13.5%
Tambient= 25°C	101	37	60	3.6	9.8%	24.5%
Tambient= 5°C	81	17	60	3.6	12.9%	41.4%
Average change in junction temperature = 5.012°C against 1°C of ambient temperature						
Average change in case temperature = 1.864°C against 1°C of ambient temperature						

Conclusion:

This research highlights the importance of thermal macro-modeling in the design and reliability of electronic circuits. Focusing on the Safe Operating Area (SOA) of MOSFETs highlights the importance of understanding and managing the thermal limits of these devices to prevent failure and maintain optimal performance. The analysis, which takes into account factors like ambient temperature, gate capacitance, and cooling methods, highlights significant findings. The findings of this study contribute to the advancement of thermal design practices, supporting the development of robust power electronic systems.

Future Work:

Future work should focus on developing advanced multi-scale thermal models that account for complex heat flow through multiple stacked layers and their interfaces. These models must incorporate variations in material properties, thermal conductance between layers, and the influence of packaging and interconnects to provide more accurate predictions. Furthermore, cooling strategies specific to 3D ICs, such as micro-channel cooling or thermally conductive substrates, need further exploration to mitigate localized heat accumulation. Integrating real-time thermal monitoring and adaptive cooling mechanisms will be essential for maintaining safe operating temperatures, improving the reliability and efficiency of high-performance electronic systems. Expanding this research to include transient thermal behavior and machine learning-based predictive models could further enhance the ability to manage thermal performance dynamically, leading to more efficient and robust power electronics designs.

References:

[1] S. Yin, T. Wang, K. J. Tseng, J. Zhao, and X. Hu, "Electro-thermal modeling of SiC power devices for circuit simulation," *IECON Proc. (Industrial Electron. Conf.*, pp. 718–723, 2013, doi: 10.1109/IECON.2013.6699223.

[2] D. P. Nayak and S. K. Pramanick, "Implementation of an Electro-Thermal Model for Junction Temperature Estimation in a SiC MOSFET Based DC/DC Converter," *CPSS Trans. Power Electron. Appl.*, vol. 8, no. 1, pp. 42–53, Mar. 2023, doi: 10.24295/CPSSTPEA.2023.00005.

[3] Z. Zhang, L. Liang, and H. Fei, "Investigation on safe-operating-area degradation and

failure modes of SiC MOSFETs under repetitive short-circuit conditions," *Power Electron. Devices Components*, vol. 4, p. 100026, Mar. 2023, doi: 10.1016/J.PEDC.2022.100026.

[4] H. Xu, X. Li, and C. Yang, "Thermal Stability Analysis of SiC MOSFET Power Modules," *2024 IEEE Int. Conf. Mechatronics Autom. ICMA 2024*, pp. 1280–1285, 2024, doi: 10.1109/ICMA61710.2024.10632947.

[5] S. Singh, J. Proulx, and A. Vass-Varnai, "Measuring the RthJC of Power Semiconductor Components Using Short Pulses," *2021 27th Int. Work. Therm. Investig. ICs Syst. THERMINIC 2021*, 2021, doi: 10.1109/THERMINIC52472.2021.9626498.

[6] "Radiation - Surface Emissivity Coefficients." Accessed: Jun. 30, 2025. [Online]. Available: https://www.engineeringtoolbox.com/radiation-heat-emissivity-d_432.html

[7] K. Heng, X. Yang, X. Wu, J. Ye, and G. Liu, "A Temperature-Dependent Physical Thermal Network Model Including Thermal Boundary Conditions for SiC MOSFET Module," *IEEE Trans. Electron Devices*, vol. 69, no. 8, pp. 4444–4452, Aug. 2022, doi: 10.1109/TED.2022.3185951.

[8] D. P. U. Tran, S. Lefebvre, and Y. Avenas, "Discrete power semiconductor losses versus junction temperature estimation based on thermal impedance curves," *IEEE Trans. Components, Packag. Manuf. Technol.*, vol. 10, no. 1, pp. 79–87, Jan. 2020, doi: 10.1109/TCPMT.2019.2939617.

[9] L. ROHM Co., "Thermal design in four steps for power devices," *ROHM*.

[10] D. Schweitzer, H. Pape, L. Chen, R. Kutscherauer, and M. Walder, "Transient dual interface measurement - A new JEDEC standard for the measurement of the junction-to-case thermal resistance," *Annu. IEEE Semicond. Therm. Meas. Manag. Symp.*, pp. 222–229, 2011, doi: 10.1109/STHERM.2011.5767204.

[11] Infineon Technologies, "IPP_B_I_200N25N3_G - Power MOSFET Data Sheet," 2016, [Online]. Available: https://www.infineon.com/dgdl/Infineon-IPP_B_I_200N25N3_G-DataSheet-v02_05-EN.pdf?fileId=db3a3043243b5f17012496b87e9f1971

[12] I. A. Technologies, "Application note Dynamic thermal behavior of MOSFETs - simulation and calculation of high power pulses", Accessed: Jul. 01, 2025. [Online]. Available: www.infineon.com

[13] X. Chen *et al.*, "Steady-state over-current safe operation area (SOA) of the SiC MOSFET at cryogenic and room temperatures," *Cryogenics (Guildf).*, vol. 122, p. 103424, Mar. 2022, doi: 10.1016/J.CRYOGENICS.2022.103424.

[14] Z. Ma *et al.*, "Characterization of Electro-Thermal Coupling Behaviors and Safe Operating Area of SiC MOSFET Modules in Pulsed Power Applications," *IEEE Trans. Power Electron.*, vol. 39, no. 9, pp. 11217–11231, 2024, doi: 10.1109/TPEL.2024.3409540.



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